

FIG. 1
(PRIOR ART)

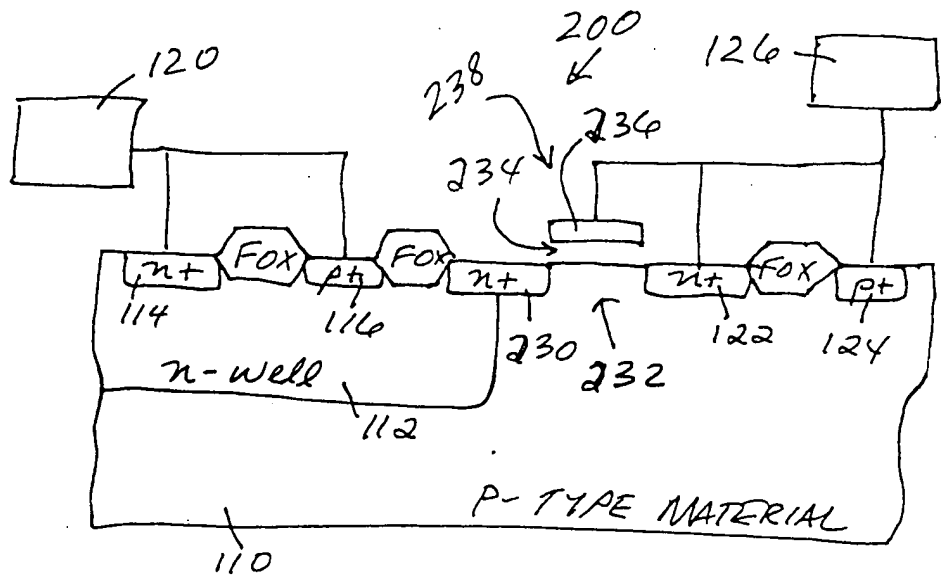


FIG. 2
(PRIOR ART)

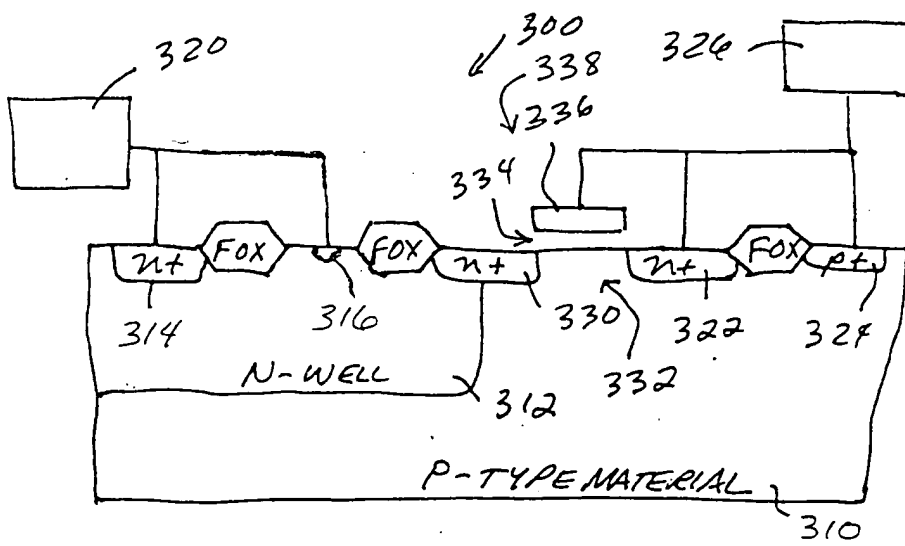


FIG. 3

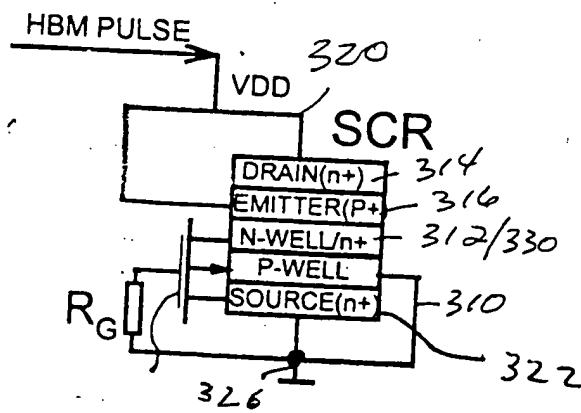


FIG. 4

TOT2E0" 4829T860

LVTSCR CMOS9DGO DEPENDENCE ON P+ REGION LENGTH AT $V_{GS}=1V$

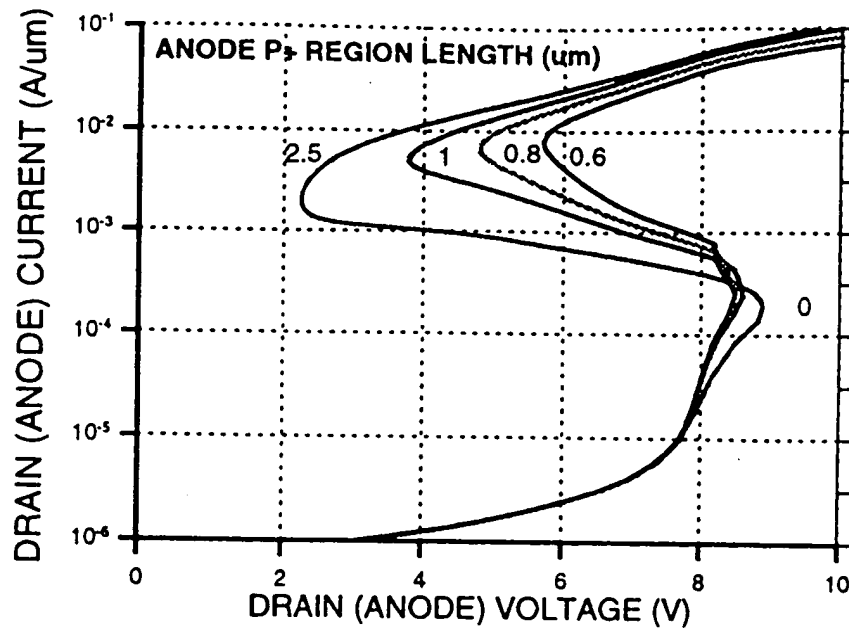


Fig 5

100ns TLP MEASUREMENTS

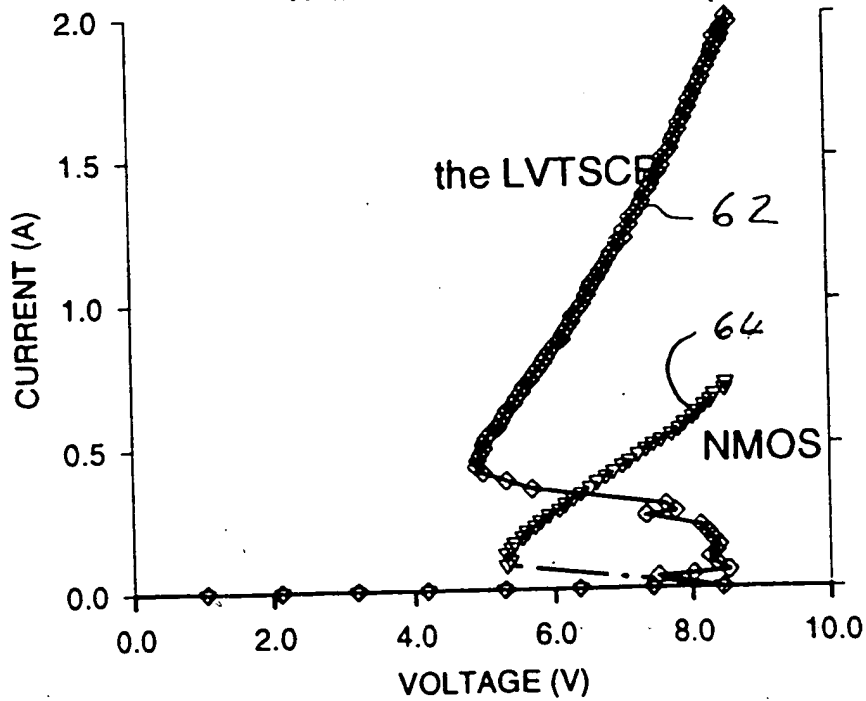


Fig 6